I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 10-2003-0071090 filed on October 13, 2003.

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Date: August 16, 2010

KOREAN INTELLECTUAL PROPERTY OFFICE

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Applicant(s):	SAMSUNG ELECTRONICS CO., LTD.

APPLICATION FOR PATENT

To the Commissioner of
the Korean Intellectual Property Office

FILING DATE: October 13, 2003

TITLE: THIN FILM TRANSISTOR, THIN FILM TRANSISTOR ARRAY PANEL, AND DISPLAY DEVICE

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Submitted herewith is an application identified above pursuant to Article 42 of the Patent Act.

[ABSTRACT OF THE DISCLOSURE]

[ABSTRACT]

A thin film transistor array panel according to the present invention includes a gate line and a data line, a thin film transistor for a gate driver and a thin film transistor for a display area. The thin film transistor for the gate driver includes a control electrode, an input electrode, an output electrode, and a channel portion between the input electrode and the output electrode, and generates a gate signal to apply it to the gate line. Also, the thin film transistor for the display area includes a gate electrode and a source electrode connected to the gate line and the data line, a drain electrode, and a channel portion between the source electrode and the drain electrode, and selectively transmits a data signal from the data line according to the gate signal from the gate line. The thin film transistor array panel includes a pixel electrode connected to the drain electrode and receiving the data signal and a shielding member disposed on the channel portion of the thin film transistor for the gate driver and made of a conductive material. The shielding member may be electrically isolated or may be applied with a negative predetermined voltage.

[REPRESENTATIVE FIGURE]

Fig. 5

[INDEX]

common electrode, threshold voltage, thin film transistor, channel

[SPECIFICATION]

[TITLE OF THE INVENTION]

THIN FILM TRANSISTOR, METHOD FOR MANUFACTURING FOR THE THIN FILM TRANSISTOR, THIN FILM TRANSISTOR ARRAY PANEL AND METHOD FOR MANUFACTURING THE THIN FILM TRANSISTOR ARRAY PANEL

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is a block diagram of a liquid crystal display according to an exemplary embodiment of the present invention.

FIG. 2 is an equivalent circuit diagram for one pixel of a liquid crystal display according to an exemplary embodiment of the present invention.

FIG. 3 is a schematic layout view showing a structure of a thin film transistor to transmit a gate-on voltage in a gate driver according to an exemplary embodiment of the present invention.

FIG. 4 is an enlarged view showing a portion of the thin film transistor shown in FIG. 3.

FIG. 5 is a cross-sectional view of the thin film transistor taken along the line V-V' of FIG. 4.

FIG. 6 is a layout view of a thin film transistor array panel for a liquid crystal display according to an exemplary embodiment of the present invention.

FIG. 7 is a cross-sectional view of the thin film transistor array panel of FIG. 6 taken along the line VII-VII'.

FIG. 8A shows a state of a liquid crystal and an equipotential line when applying a common voltage of +3.3V to a common electrode.

FIG. 8B shows a state of a liquid crystal and an equipotential line when applying a common voltage of -1.0V to a common electrode.

FIG. 8C shows a state of a liquid crystal and an equipotential line when removing a common electrode.

FIG. 9A and FIG. 10A show a variation of a gate signal output from a gate driver when respectively applying a common voltage of +3.3V and -1.0V in a state that a liquid crystal layer is not removed.

FIG. 9B and FIG. 10B show a variation of a gate signal output from a gate driver when respectively applying a common voltage of +3.3V and -1.0V in a state that a liquid crystal layer is removed.

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND CONVENTIONAL ART IN THE FIELD]

The present invention relates to a thin film transistor, a manufacturing method of a thin film transistor, a thin film transistor array panel, and a manufacturing method of a thin film transistor.

A liquid crystal display (LCD) generally includes two panels provided with pixel electrodes and a common electrode, and a liquid crystal (LC) layer with dielectric anisotropy disposed between the panels. The pixel electrodes are arranged in a matrix and are connected to switching elements such as thin film transistors (TFTs) such that they are supplied with data voltages row by row in a sequential manner. The common electrode covers an entire surface of one of the panels and is supplied with a common voltage. A pixel electrode and a common electrode as well as a LC layer interposed therebetween form an LC capacitor, and the LC capacitor and a switching element connected thereto are the basic elements of a pixel.

The LCD applies voltages to the electrodes to form an electric field in the LC layer and adjusts the field strength to control transmittance of light passing through the LC layer, thereby realizing desired images on the display.

This liquid crystal display which is representative of portable flat panel displays (FPDs) includes a plurality of gate lines and a plurality of data lines that are connected to the switching element, and each gate line transmits a gate-on voltage turning-on the switching element, and each data line transmits the data voltage to each pixel through the turned-on switching element. Also, the liquid crystal display includes a gate driver applying the gate-on voltage to the gate line, a data driver applying the data voltage to the data line, and a signal controller controlling them, and the gate driver and the data driver include a plurality of gate driving ICs(integrated circuits) and a plurality of data driving ICs.

The plurality of gate drivers IC or the plurality of data drivers IC may be directly attached on the glass substrate (chip on glass, COG mounting type), may be mounted on a TCP(tape carrier package) (not shown) and the TCP may be attached to the display panel.

Also, for a narrow bezel requirement that an effective screen is expanded and an area of an external frame of the screen is decreased, and a cost reduction, the gate driver is recently formed along with the switching element to integrate the gate driver on the same substrate [GIL(gate IC less) structure].

[TECHNICAL TASK OF THE INVENTION]

In general, a switching element formed in a lower panel of a liquid crystal display is affected by a common voltage applied to a common electrode of an upper panel as following.

When applying the common voltage to the upper panel, an actual threshold voltage (Vt) may be represented as [Equation 1].

(Equation 1)

$$Vt = Vto + \gamma[\sqrt{(2\phi f + Vcs)} - \sqrt{(2\phi f)}]$$

Here, Vt: th threshold voltage, Vto: th threshold voltage when Vcs=0, γ: a manufacturing process parameter, ø: a constant, Vcs=Vc-Vs(Vc: the common voltage, Vs: a voltage applied to a source electrode of the thin film transistor)

As shown in [Equation 1], the actual threshold voltage(Vt) is proportional to the value of Vcs, the source voltage supplied to the source electrode is the data voltage applied from the data driver, thus the actual threshold voltage(Vt) is substantially proportional to the value of the common voltage Vcom.

As above described, the actual threshold voltage(Vt) is changed according to the common voltage Vcom such that it is generated that the driving voltage applied to the gate electrode of the thin film transistor is decreased when the actual threshold voltage(Vt) is decreased, thereby the turn-on time of the thin film transistor is low, and the current flow of the turn-on time is increased, resultantly the operation efficiency of the thin film transistor is increased.

However, when the actual threshold voltage(Vt) is increased, the driving voltage applied to the gate electrode is increased such that the turn-on time of the thin film transistor is high, and the current flow of the turn-on time is decreased, resultantly the operation efficiency of the thin film transistor is decreased.

Also, when the gate signal is applied through the gate electrode, a capacitor is formed between the common electrode and the gate electrode, and the gate-on voltage of the applied gate signal is decreased by the capacitor. Accordingly, the problem that the gate-on voltage for the channel formation between the source electrode and the drain electrode is generated.

Furthermore, the switching element formed in the gate driver region in the GIL structure has the considerably larger size than the switching element formed in the pixel area such that the channel width is considerably large in the degree of 7000 to 10000μm. As above described, as the channel width of the switching element is increased, the influence of the capacitor formed between the common electrode and the gate electrode is large.

Actually comparing the capacitor(C_{gs}) formed between the gate electrode and the source electrode and the capacitor(C_{gc}) formed between the gate electrode and the common electrode,

C_{gs}:C_{gc} = 4.6:1(with reference to a low voltage liquid crystal)

The capacitance of the capacitor C_{gc} is very large to have the effect on the driving of the liquid crystal display.

Accordingly, a technical object according to the present invention decreases the bad influence to the switching element from the common voltage applied to the upper panel of the liquid crystal display.

Also, another technical object according to the present invention prevents the unnecessary voltage loss and improves the driving voltage efficiency of the liquid crystal display by substantially generating the reduction effect of the threshold voltage of the switching element.

[CONFIGURATION AND OPERATION OF THE INVENTION]

A thin film transistor according to the present invention includes

a gate electrode,

a gate insulating layer formed on the gate electrode,

a semiconductor layer formed on the gate insulating layer,

a source electrode and a drain electrode formed on at least portion of the semiconductor layer and facing to each other,

a passivation layer formed on the source electrode, the drain electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and

a shielding member formed on the passivation layer, disposed between the source electrode and the drain electrode, and made of a conductive material.

It is preferable that the shielding member is electrically isolated or applied with a predetermined voltage, here, the predetermined voltage is a negative voltage. Also, the shielding member is formed with the same layer as the pixel electrode.

It is preferable that the shielding member is made of IZO or ITO, the shielding member has a horseshoes.

A thin film transistor array panel according to the present invention includes

a gate line and a data line,

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode, and generating a gate signal to apply it to the gate line,

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode, and selectively transmitting a data signal from the data line according to the gate signal from the gate line,

a pixel electrode connected to the drain electrode and receiving the data signal, and

a first shielding member disposed on the channel portion of the first thin film transistor and made of a conductive material.

It is preferable that the first shielding member is electrically isolated or applied with a predetermined voltage, here, the predetermined voltage is a negative voltage.

A liquid crystal display according to the present invention includes

a first display panel including a plurality of gate line and data line,

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel layer, and generating a gate signal to apply it to the gate line,

a second thin film transistor selectively transmitting a data signal from the data line according to the gate signal from the gate line,

a pixel electrode connected to the second thin film transistor receiving the data signal, and

a shielding member formed on the channel layer of the first thin film transistor and made of a conductive material,

a second display panel having a common electrode, and

a liquid crystal layer disposed between the first and the second display panels, aligned according to an electric field generated by the common electrode and the pixel electrode.

Also, the first shielding member may be formed with the same layer as the pixel electrode.

The common electrode may face the shielding member.

A manufacturing method of a thin film transistor according to the present invention includes

forming a gate electrode on a substrate,

forming a gate insulating layer on the gate electrode,

forming a semiconductor layer on the gate insulating layer,

forming a source electrode and a drain electrode on at least portion of the semiconductor layer,

forming a passivation layer on the source electrode, the drain electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and

forming a shielding member on the semiconductor layer between the source electrode and the drain electrode, and made of a conductive material.

The shielding member may be made of IZO or ITO.

A manufacturing method of a thin film transistor array panel according to the present invention includes

forming a gate electrode and a control electrode on a substrate,

forming a gate insulating layer on the gate electrode and the control electrode,

forming a semiconductor layer on the gate insulating layer,

forming a source electrode and a drain electrode contacted with the semiconductor layer, and an input electrode and an output electrode,

forming a passivation layer on the source electrode and the drain electrode, and the input electrode and the output electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and the input electrode and the output electrode,

forming a pixel electrode on the passivation layer, and

forming a first shielding member made of a conductive material on the passivation layer between the input electrode and the output electrode.

It is preferable that the pixel electrode and the first shielding member are simultaneously formed.

The manufacturing method of the thin film transistor array panel may further include forming a second shielding member on the passivation layer between the source electrode and the drain electrode.

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Then, a liquid crystal display according to embodiments of the present invention will be described with reference to the accompanying drawings.

FIG. 1 is a block diagram of a liquid crystal display according to an exemplary embodiment of the present invention, and FIG. 2 is an equivalent circuit diagram for one pixel of a liquid crystal display according to an exemplary embodiment of the present invention.

Referring to Fig. 1, a liquid crystal display according to an embodiment includes a liquid crystal panel assembly 300, a gate driver 400 and a data driver 500 that are connected thereto, a gray signal generator 800 connected to the data driver 500, and a signal controller 600 controlling the above elements.

In a view point of an equivalent circuit, the liquid crystal panel assembly 300 includes a plurality of display signal lines G_1-G_n and D_1-D_m and a plurality of pixels PX connected thereto and arranged substantially in a matrix.

The display signal lines G_1-G_n and D_1-D_m include a plurality of gate lines G_1-G_n transmitting gate signals (also referred to as "scanning signals"), and a plurality of data lines D_1-D_m transmitting data signals. The gate lines G_1-G_n extend substantially in a row direction and substantially parallel to each other, while the data lines D_1-D_m extend substantially in a column direction and substantially parallel to each other.

Each pixel includes a switching element Q connected to the display signal lines G_1-G_n and D_1-D_m and a liquid crystal capacitor C_{LC} and a storage capacitor C_{ST} connected thereto. The storage capacitor C_{ST} may be omitted, if necessary.

The switching element Q provided on the lower panel 100 and having three terminals: a control terminal connected to one of the gate lines G_1-G_n; an input terminal connected to one of the data lines D_1-D_m; and an output terminal connected to both the LC capacitor C_{LC} and the storage capacitor C_{ST}.

The LC capacitor C_{LC} includes a pixel electrode 190 provided on the lower panel 100 and a common electrode 270 provided on the upper panel (referred to as "a color filter array panel") 200 as two terminals. The LC layer 3 disposed between the two electrodes 190 and 270 functions as dielectric of the LC capacitor C_{LC}.. The pixel electrode 190 is connected to the switching element Q, and the common electrode 270 is supplied with a common voltage Vcom and covers an entire surface of the upper panel 200. Unlike Fig. 2, the common electrode 270 may be provided on the lower panel 100, and both electrodes 190 and 270 may have shapes of bars or stripes.

The storage capacitor C_{ST} includes the pixel electrode 190 and a separate signal line, which is provided on the lower panel 100, overlaps the pixel electrode 190 via an insulator, and is supplied with a predetermined voltage such as the common voltage Vcom. Alternatively, the storage capacitor C_{ST} includes the pixel electrode 190 and a previous gate line, which overlaps the pixel electrode 190 via an insulator.

For color display, each pixel PX may represents one of colors, and it is possible to provide color filters 230 of red, green, or blue on the region corresponding to the pixel electrode 190. In FIG. 2, the color filter 230 is formed on the corresponding region of the upper panel 200, however the color filter 230 may be provided on or under the pixel electrode 190 on the lower panel 100.

One or more polarizers (not shown) for the polarization are attached to at least one of the panels 100 and 200 of the liquid crystal panel assembly 300.

The gray signal generator 800 generates two sets of a plurality of gray voltages related to the transmittance of the pixels PX. The gray voltages in one set have a positive polarity with respect to the common voltage Vcom, while those in the other set have a negative polarity with respect to the common voltage Vcom.

The gate driver 400 is connected to the gate lines G_1-G_n of the liquid crystal panel assembly 300 and applies gate signals with the combination of a gate-on voltage Von and a gate-off voltage Voff. The gate driver 400 may include a plurality of integrated circuits IC. The IC of the gate driver 400 according to an exemplary embodiment of the present invention has the structure (the GIL structure) that the circuit executing the function as shown in FIG. 1 is directly mounted to the liquid crystal panel assembly 300. The most of the plurality of circuits forming the gate driver 400 are the switching elements including the thin film transistor. In general, ach of the driving circuits is connected to one of the gate lines G_1-G_n and includes about fourteen thin film transistors.

FIG. 3 shows the thin film transistor transmitting the gate-on voltage Von to the corresponding gate lines G_1-G_n. As shown in FIG. 3, the thin film transistor is supplied with the source voltage from an external through the input signal line 171a, and receives the driving signal through the control signal line 126. Accordingly, if the driving signal is applied through the control signal line 126, the thin film transistor is turned-on, the current of the source voltage supplied through the input signal line 171a flows through the turned-on thin film transistor, thereby the gate-on voltage Von is output to the output signal line 176 and is transmitted to the corresponding gate lines G_1-G_n. The voltages such as the source voltage and the driving signal, or the control signal are supplied from the signal controller 600 through a plurality of signal lines (not shown) formed on the left side of the gate driver 400 on the liquid crystal panel assembly 300.

The data driver 500 is connected to the data lines D_1-D_m of the liquid crystal panel assembly 300 and selects the gray voltage from the gray voltage generator 800 to apply it as the data signal to the pixel, and the data driver 500 includes a plurality of ICs.

In an exemplary embodiment of the present invention, the gate driver 400 is directly integrated to the liquid crystal panel assembly 300, however a plurality of gate drivers IC or data drivers IC are directly attached on the glass substrate in forms of IC chips (chip on glass, a COG mount type), or may be mounted to a TCP(tape carrier package) (not shown) and then the TCP is attached to liquid crystal panel assembly 300.

The signal controller 600 generates a control signal controlling the operation of the gate driver 400 and the data driver 500, and provides the corresponding control signal to the gate driver 400 and the data driver 500.

Next, a structure of a liquid crystal display according to an exemplary embodiment of the present invention will be described with reference to FIG. 3 to FIG. 7.

FIG. 3 is a schematic layout view showing a structure of a thin film transistor to transmit a gate-on voltage in a gate driver according to an exemplary embodiment of the present invention, FIG. 4 is an enlarged view showing a portion of the thin film transistor shown in FIG. 3, and FIG. 5 is a cross-sectional view of the thin film transistor taken along the line V-V' of FIG. 4. FIG. 6 is a layout view of a thin film transistor array panel for a liquid crystal display according to an exemplary embodiment of the present invention, FIG. 7 is a cross-sectional view of the thin film transistor array panel of FIG. 6 taken along the line VII-VII'.

FIG. 5 is a cross-sectional view of the gate driver region among the liquid crystal display, and FIG. 7 a cross-sectional view of the display area among the liquid crystal display.

Firstly, a structure of a region of the gate driver 400 among the lower panel 100 and the upper panel 200 of the liquid crystal display and the upper panel(color filter array panel) 200 of the display area will be described with reference to FIG. 5 and FIG. 7.

The upper panel 200 includes a transparent insulation substrate 210, and a black matrix 220 formed on the insulation substrate 210. The black matrix 220 formed in the display area has a plurality of openings defining the pixel areas, while the black matrix 220 formed on the region of the gate driver 400 does not have a separate opening. Also, the upper panel 200 includes the color filter 230 of red, green and blue formed in the pixel area of the display area, an overcoat 250 formed on the color filter 230, a common electrode 270 formed on the overcoat 250, and an alignment layer 21 formed on the common electrode 270. The pixel area is not defined on the region of the gate driver 400 such that the color filter 230 is not formed, and the alignment layer 21 may be made of polyimide.

In an exemplary embodiment of the present invention, the thickness of the liquid crystal layer 3, or the interval is about 3.7μm, and the thickness of the color filter is in the range of about 1.5μm to 1.6μm.

Next, a structure of the thin film transistor array panel of the liquid crystal display will be described.

A plurality of gate lines 121 transmitting gate signals and a control signal line 126 are formed on the insulation substrate 110. The gate line 121 and the control signal line 126 mainly extend in a horizontal direction, and the portion of each gate line 121 forms a plurality of gate electrodes 124. Also, the other portion of each gate line extends in a low direction thereby forming a plurality of expansions 127. The portion of the control signal line 126 forms a control electrode 124a.

The gate lines 121 and the control signal lines 126 are preferably made of a conductive layer having low resistivity such as Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy. However, the gate lines 121 and the control signal lines 126 may have a multi-layered structure including the other layer made of material such as Mo containing metal, Cr, Ta, Ti, and alloys thereof(for example, molybdenum-tungsten(MoW) alloy), which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) and indium zinc oxide (IZO). An example of the combination of the lower layer and the upper layer may be chromium/aluminum-neodymium(Nd) alloy.

The lateral sides of the gate lines 121 and the control signal line 126 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 30-80 degrees.

A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121 and the control signal lines 126.

A plurality of semiconductor islands 154 and 155 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon are formed on the gate insulating layer 140 of the gate electrode 124 and the control electrode 124a.

A plurality of pairs of ohmic contact islands 163 and 165 and other pairs of ohmic contact islands 163a and 165a preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor islands 154 and 155, respectively.

The lateral sides of the semiconductor islands 154 and 155 and the ohmic contacts 163 and 165, and 163a and 165a are inclined relative to a surface of the substrate 110, and the inclination angles thereof are preferably in a range of about 30-80 degrees.

A plurality of data lines 171, a plurality of input signal lines 171a, a plurality of drain electrodes 175, a plurality of output signal lines 176, and a plurality of storage capacitor conductors 177 are formed on the ohmic contacts 163, 165, 163a and 165a and the gate insulating layer 140.

The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. Each data line 171 includes A plurality of branches projecting toward the drain electrodes 175 to form a plurality of source electrodes 173. Each pair of the source electrodes 173 and the drain electrodes 175 are separated from each other and opposite each other with respect to a gate electrode 124.

The input signal line 171a includes a portion mainly extending in the vertical direction, a plurality of main branches in the horizontal direction from the signal line 171a, that is, three main branches from the predetermined portion of the signal line 171a thereby forming an input signal line connection 172. The input signal line connection 172 includes a plurality of branches with a comb shape of an uniform interval in the vertical direction, thereby forming an input electrode 173a.

Also, the output signal line 176 includes a portion mainly extending in the vertical direction, and two main branches extending from the predetermined portion of the signal line 176 in the horizontal direction thereby forming an output signal connection 178. A plurality of branches are formed with an uniform interval in the vertical direction on the both sides of the output signal line connection 178 thereby forming an output electrode 175a.

A gate electrode 124 and a control electrode 124a, a source electrode 173 and an input electrode 173a, and a drain electrode 175 and an output electrode 175a respectively form a thin film transistor(TFT) along with the semiconductors 154 and 155, and the channel of the thin film transistor is respectively formed in the semiconductors 154 and 155 between the source electrode 173 and the input electrode 173a, and the drain electrode 175 and the output electrode 175a. The output electrode 175a is alternately arranged along with the input electrode 173a of the output signal line 176 such that the channel formed between the input electrode 173a and the output electrode 175a has a shape of horseshoes.

The storage capacitor conductor 177 overlaps the expansion 127 of the gate line 121.

The data lines 171, the input signal lines 171a, the drain electrodes 175, the output signal lines 176, and the storage capacitor conductors 177 are preferably made of a conductive layer

having low resistivity such as Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy. However, they may have a multi-layered structure including the other layer made of material such as Mo containing metal, Cr, Ta, Ti, and alloys thereof(for example, molybdenum-tungsten(MoW) alloy), which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) and indium zinc oxide (IZO). An example of the combination of the lower layer and the upper layer may be chromium/aluminum-neodymium(Nd) alloy.

The lateral sides of the data lines 171, the input signal lines 171a, the drain electrodes 175, the output signal lines 176, and the storage capacitor conductors 177 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 30-80 degrees.

The ohmic contacts 163, 165, 163a and 165a are interposed only between the underlying semiconductor islands 154 and 155 and overlying layers including the data lines 171, the drain electrodes 175, and the input and the output signal lines 171a and 176 and reduce the contact resistance therebetween.

A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, the input and the output signal lines 171a and 176, the storage electrode capacitors 177, and exposed portions of the semiconductor islands 154, which are not covered with the data lines 171, etc. The passivation layer 180 is preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma-enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride. The passivation layer 180 may have a double-layered structure including silicon nitride film and the organic material film.

The passivation layer 180 has a plurality of contact holes 182, 185 and 187 exposing the end portions 179 of the data lines 171, the drain electrodes 175, and the storage conductors 177, respectively.

A plurality of pixel electrodes 190, a plurality of shielding members 196 and 196a, and a plurality of contact assistants 82, which are preferably made of transparent conductive material such as ITO or IZO, are formed on the passivation layer 180.

The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 185 and to the storage capacitor conductors 177 through the contact

holes 187 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175 and transmit the received data voltages to the storage capacitor conductors 177.

The shielding member 196 is formed on the channel portion between the drain electrode 175 and the output electrode 175a, and the source electrode 173 and the input electrode 173a. The shielding electrodes 196 formed the output electrode 175a and the input electrode 173a has the shape of horseshoe, and receives the gate-off voltage Voff applied from the external through a signal line(not shown). In an exemplary embodiment of the present invention, the shielding member 196 is applied with the gate-off voltage Voff, however any voltage may be not applied, and a ground voltage may be applied except for the gate-off voltage Voff.

Again referring to FIG. 2, the pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with the common electrode 270 on the upper panel 200, which rearrange liquid crystal molecules in the liquid crystal layer 3 between two electrodes 190 and 270.

As described above, a pixel electrode 190 and the common electrode 270 form a liquid crystal capacitor, which maintains the applied voltage after a turn-off of the thin film transistor. The other capacitor for enhancing the voltage storing capacity is coupled in parallel to the liquid crystal capacitor and the other capacitor is referred to as a storage capacitor". The storage capacitor C_{ST} is implemented by overlapping the pixel electrode 190 with the gate line 121 adjacent thereto(referred to as a previous gate line. The capacitances of the storage capacitors, i.e., the storage capacitances are increased by providing the projections 127 extended from the gate lines 121 for increasing overlapping areas and by providing the storage capacitor conductors 177, which are connected to the pixel electrodes 190 and overlap the projections 127, under the passivation layer 180 for decreasing the distance between the terminals.

The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase aperture ratio but it is optional.

The contact assistants 82 are connected to the exposed end portions 179 of the data lines 171 through the contact holes 182, respectively. The contact assistants 82 protect the exposed end portions 179 and complement the adhesion between the end portions 179 and external devices, but it is optional.

According to another exemplary embodiment of the present invention, the pixel electrodes 190 are made of transparent conductive polymer. For a reflective LCD, the pixel electrodes 190 are made of opaque reflective metal. In these cases, the contact assistants 82 may be made of material such as ITO or IZO different from the pixel electrodes 190.

An alignment layer 11 preferably made of polyimide is coated on the pixel electrodes 190, the shielding electrode 196, and portions of the passivation layer 180 that are not covered with the pixel electrodes 190 and the shielding electrodes 196.

As above described, the shielding electrodes 196 on the channels of the TFTs block the effect of the common voltage Vcom applied to the common electrode 270 on the liquid crystal layer 3 or the other electrode to prevent the deterioration of the threshold voltage of the TFTs. In addition, in an exemplary embodiment of the present invention, the gate-off voltage Voff is applied to the shielding member 1960 such that the voltage difference between the gate electrode and the shielding member 196 is further increased, accordingly a driving voltage of the TFTs is reduced and advances the switching time of the TFTs, thereby increasing the efficiency of the gate-on voltage and the efficiency of the operation of the TFTs.

Now, the display operation of the above-described liquid crystal display will be described in detail.

The signal controller 600 is supplied with input image signals R, G and B and input control signals controlling the display thereof such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a main clock MCLK, and a data enable signal DE, from an external graphics controller (not shown). After generating gate control signals CONT1 and data control signals CONT2 and processing the input image signals R, G and B suitable for the operation of the liquid crystal panel assembly 300 on the basis of the input control signals and the input image signals R, G and B, the signal controller 600 transmits the gate control signals CONT1 to the gate driver 400, and the processed image signal R′, G′ and B′ and the data control signals CONT2 to the data driver 500.

The gate control signals CONT1 include a scanning start signal STV for instructing to output start of the gate-on pulse(the high period of the gate signal), a gate clock signal CPV for controlling the output time of the gate-on plus, an output enable signal OE for defining the width of the gate-on pulse.

The data control signals CONT2 include a horizontal synchronization start signal STH for instructing to input start of the image data R', G' and B', a load signal LOAD for instructing to apply the data voltages to the data lines D_1-D_m, a inversion control signal RVS for reversing the polarity of the data voltages (with respect to the common voltage Vcom), and a data clock signal HCLK.

The data driver 500 sequentially receives the image data R', G' and B' for a pixel row according to the data control signal CONT2 from the signal controller 600 and select the gray voltages corresponding to the image data R', G' and B' among the gray signals from the gray signal generator 800 to convert the image data R', G' and B' into the corresponding data voltage.

The gate driver 400 applies the gate-on voltage Von to the gate lines G_1-G_n according to the gate control signal CONT1 from the signal controller 600 to turn-on the switching element Q connected to the gate lines G_1-G_n.

The data driver 500 supplies the data voltage to the corresponding data lines D_1-D_m during the time that one of the gate lines G_1-G_n is applied with the gate-on voltage Von such that the switching elements Q connected thereto of one row are turned-on [this period is referred to as "1H" or "1 horizontal period and equal to one period of the horizontal synchronizing signal Hsync, the data enable signal DE, the gate clock CPV]. The data voltage supplied to the data lines D_1-D_m is applied to the corresponding pixel through the turned-on switching element Q.

By this method, the gate-on voltage Von are sequentially applied to all gate lines G_1-G_n during one frame to apply the data voltage to all pixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver 500 is controlled such that the polarity of the data voltages is reversed (which is called "frame inversion").. The inversion control signal RVS may be also controlled such that the polarity of the data voltages flowing in a data line in one frame are reversed (line inversion and dot inversion), or the polarity of the data voltages in one pixel row are reversed (dot inversion).

Next, a variation of a liquid crystal and an equipotential line according to a variation of a common voltage Vcom applied to the common electrode 270 will be described with reference to FIG. 8. FIG. 8A to FIG. 8C are views showing a variation of a liquid crystal and an equipotential line according to a variation of a common voltage Vcom.

FIG. 8A shows a state of a liquid crystal and an equipotential line when applying a common voltage of +3.3V to a common electrode 270, FIG. 8B shows a state of a liquid crystal and an equipotential line when applying a common voltage of -1.0V to a common electrode 270, and FIG. 8C shows a state of a liquid crystal and an equipotential line when removing a common electrode.

As shown in FIG. 8A and FIG. 8B, as the common voltage Vcom applied to the common electrode 270 is increased, the effect of the common voltage Vcom on the drain voltage and the source voltage respectively applied to the drain electrode and the source electrode is large such that the equipotential line is formed parallel to the upper panel 200 applied with the common voltage Vcom. However, as shown in FIG. 8C, when the common electrode is removed such that the common voltage Vcom is not applied to the upper display unit 200, the equipotential line is determined by the effect of the drain voltage and the source voltage such that the arrangement of the liquid crystal molecule is determined. Here, the electromagnet influenced to the arrangement of the liquid crystal molecule is operated in the direction vertical to the equipotential line.

As previously described, as the value of the common voltage Vcom applied to the common electrode is decreased, it is generated that the threshold voltage of the thin film transistor is decreased, thereby it may be confirmed that the operation efficiency of the thin film transistor is improved as the common voltage Vcom of the small value is applied.

Next, a variation of a gate signal output from a gate driver according to a variation of a common voltage Vcom will be described with reference to FIG. 9A and FIG. 9B and FIG. 10A and FIG. 10B.

FIG. 9A shows a variation of a gate signal output from a gate driver when respectively applying a common voltage of +3.3V in a state that a liquid crystal layer 3 is not removed, and FIG. 9B shows a variation of a gate signal output from a gate driver when respectively applying a common voltage of +3.3V in a state that a liquid crystal layer s is removed.

Also, FIG. 10A shows a variation of a gate signal output from a gate driver when respectively applying a common voltage of -1.0V in a state that a liquid crystal layer 3 is not removed, and FIG. 10B shows a variation of a gate signal output from a gate driver when respectively applying a common voltage of -1.0V in a state that a liquid crystal layer s is removed.

When the liquid crystal layer 3 is not removed, if the gate signal of +23.6V is applied to the gate driver 400, in the case of FIG. 9A, the gate signal of about +14.6V is output such that the voltage drop of about 9.0V is generated, however, in the case of FIG. 10A, the gate signal of about +20.6V is output such that the voltage drop of about 3.0V is only generated. Like this, as the value of the common voltage Vcom is decreased, the influence of the liquid crystal layer 3 and the gate electrode by the common voltage is decreased such that the voltage drop of the gate signal output from the gate driver 400 and applied to the corresponding gate lines G_1-G_n is decreased, thereby the operation efficiency of the thin film transistor is improved.

FIG. 9B and FIG. 10B show the variation of the gate signal output when the liquid crystal layer is remover and the gate signal of +23.6V is applied to the gate driver 400, and there is a state that the influence of the liquid crystal layer 3 for the common voltage Vcom is not existed such that the gate signal output as +20.6V and +20.8V does not have the difference in the cases that the common voltage Vcom of +3.3V is applied, or the common voltage Vcom of -1.0V is applied.

While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

[ADVANTAGE OF THE INVENTION]

As above described, the present invention forms the shielding member on the channel portion to prevent the influence from the common voltage applied to the common electrode of the upper panel for the operation of the thin film transistor formed on the lower panel of the liquid crystal display. Accordingly, the increasing of the threshold voltage by the common voltage may be prevented, and the capacitance of the capacitor generated between the common electrode and the gate electrode may be reduced, thereby the operation efficiency of the thin film transistor may be increased, and the unnecessary loss of the gate-on voltage may be prevented.

Also, the shielding member is applied with the voltage(-) such as the gate-off voltage, and the voltage difference between the shielding member and the gate electrode is largely increased, resultantly the threshold voltage of the thin film transistor is largely decreased, thereby the operation efficiency of the thin film transistor and the efficiency of the driving voltage are largely improved.

Furthermore, the shielding member is formed with the same layer as the pixel electrode such that the additional mask or the additional process is not necessary, thereby the manufacturing cost is not increased, and the manufacturing process is not increased.

[CLAIMS]

1. A thin film transistor comprising:

a gate electrode,

a gate insulating layer formed on the gate electrode,

a semiconductor layer formed on the gate insulating layer,

a source electrode and a drain electrode formed on at least portion of the semiconductor layer and facing to each other,

a passivation layer formed on the source electrode, the drain electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and

a shielding member formed on the passivation layer, disposed between the source electrode and the drain electrode, and made of a conductive material.

2. The thin film transistor of claim 1, wherein:
the shielding member is electrically isolated.

3. The thin film transistor of claim 1, wherein:
the shielding member is applied with a predetermined voltage.

4. The thin film transistor of claim 3, wherein:
the predetermined voltage is a negative voltage.

5. The thin film transistor of claim 1, wherein:
the shielding member is made of IZO or ITO.

6. The thin film transistor of claim 1, wherein:
the shielding member has a horseshoes.

7. The thin film transistor of claim 1, wherein:
the passivation layer is made of an organic insulating material.

8. A thin film transistor array panel comprising:

a gate line and a data line,

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel portion disposed between the input electrode and the output electrode, and generating a gate signal to apply it to the gate line,

a second thin film transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, a drain electrode, and a channel portion disposed between the source electrode and the drain electrode, and selectively transmitting a data signal from the data line according to the gate signal from the gate line,

a pixel electrode connected to the drain electrode and receiving the data signal, and

a first shielding member disposed on the channel portion of the first thin film transistor and made of a conductive material.

9. The thin film transistor array panel of claim 8, wherein:

the first shielding member is electrically isolated.

10. The thin film transistor array panel of claim 8, wherein:

the first shielding member is applied with a predetermined voltage.

11. The thin film transistor array panel of claim 10, wherein:

the predetermined voltage is a negative voltage.

12. The thin film transistor array panel of claim 8, wherein:

the first shielding member is formed with the same layer as the pixel electrode.

13. The thin film transistor array panel of claim 8, further comprising:

a second shielding member formed on a channel portion of the second thin film transistor and formed with the same layer as the pixel electrode.

14. The thin film transistor array panel of claim 13, further comprising:

a passivation layer formed between the source electrode, the drain electrode and the channel portions of the first and the second thin film transistors, and the first and the second shielding member and the pixel electrode.

15. The thin film transistor array panel of claim 14, wherein:

the passivation layer is made of an organic insulating material.

16. A liquid crystal display comprising:

a first display panel including a plurality of gate line and data line,

a first thin film transistor including a control electrode, an input electrode, an output electrode, and a channel layer, and generating a gate signal to apply it to the gate line,

a second thin film transistor selectively transmitting a data signal from the data line according to the gate signal from the gate line,

a pixel electrode connected to the second thin film transistor receiving the data signal, and

a shielding member formed on the channel layer of the first thin film transistor and made of a conductive material,

a second display panel having a common electrode, and

a liquid crystal layer disposed between the first and the second display panels, aligned according to an electric field generated by the common electrode and the pixel electrode.

17. The liquid crystal display of claim 16, wherein:

the shielding member is formed with the same layer as the pixel electrode.

18. The liquid crystal display of claim 17, wherein:

the common electrode faces the shielding member.

19. A manufacturing method of a thin film transistor comprising:

forming a gate electrode on a substrate,

forming a gate insulating layer on the gate electrode,

forming a semiconductor layer on the gate insulating layer,

forming a source electrode and a drain electrode on at least portion of the semiconductor layer,

forming a passivation layer on the source electrode, the drain electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and

forming a shielding member on the semiconductor layer between the source electrode and the drain electrode, and made of a conductive material.

20. The method of claim 19, wherein:

the shielding member is made of IZO or ITO.

21. A manufacturing method of a thin film transistor array panel comprising:

forming a gate electrode and a control electrode on a substrate,

forming a gate insulating layer on the gate electrode and the control electrode,

forming a semiconductor layer on the gate insulating layer,

forming a source electrode and a drain electrode contacted with the semiconductor layer, and an input electrode and an output electrode,

forming a passivation layer on the source electrode and the drain electrode, and the input electrode and the output electrode, and the semiconductor layer that is not covered by the source electrode and the drain electrode, and the input electrode and the output electrode,

forming a pixel electrode on the passivation layer, and

forming a first shielding member made of a conductive material on the passivation layer between the input electrode and the output electrode.

22. The method of claim 21, wherein:

the pixel electrode and the first shielding member are simultaneously formed.

23. The method of claim 21, wherein:

the passivation layer is made of an organic insulating material.

24. The method of claim 21, wherein:

the pixel electrode is made of IZO or ITO.

25. The method of claim 21, further comprising,

forming a second shielding member on the passivation layer between the source electrode and the drain electrode.